Remarks

Claims 1-20 are pending in this application. The examiner has rejected claims 1-20 as being obvious under 35 U.S.C. § 103 over U.S. Patent No. 6,282,601 to Goodman et al, in view of U.S. Patent No. 5,692,197 to Narad et al.

A. Independent Claims 1 and 15

The Examiner recognizes that Goodman does not disclose all of the elements of the claimed invention. In particular, the Examiner recognizes that Goodman does not disclose the following step of independent claims 1 and 15:

> wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

(Claims 1 and 15). The element provides that each of the processors can enter an interrupt mode, and memory includes a uniquely addressable semaphore for each processor that identifies when the associated processor has exited interrupt mode.

The examiner, however, finds the teaching for this element in the following passage of Narad, which is provided in its entirety below:

> S_Sleep_Enter and S_Wakeup_Enable semaphore bits: the S_Sleep_Enter semaphore bit of the system controller provides an indicator that the computer system is in the process of entering the sleep state, and inhibits power up of the processor module(s) until the corresponding S_Wakeup_Enable semaphore bit is set. The setting of the S_Wakeup_Enable bit indicates that the processor module(s) of the computer system has completed the power-down sequence and it is now safe to initiate a power up of the processor module(s).
>
> Wakeup_Reset bit: a status bit of the system controller for indicating that the cause of reset signal is a wakeup of the computer system, as opposed to a system-wide power on reset.

(Narad, col. 4, lines 8-22). This passage of Narad, and the entirety of Narad, plainly do not disclose the semaphore step of claims 1 and 15.

First, Narad is directed to computer systems. Claims 1 and 15 are directed to processors. Second, Narad says nothing about the presence of a uniquely addressable semaphore in memory. There is no mention in Narad of the storage location of the bits of Narad or whether the bits of Narad include bits that are uniquely associated with each one of the computer systems of Narad.

Finally, the semaphores that are disclosed in Narad do not indicate when a processor of the system has exited interrupt mode. Rather, the semaphores of Narad indicate (a) when a processor is entering a sleep state and (b) when a processor is in a sleep state. Narad plainly does not disclose a set of semaphores that identify when a processor has exited *an interrupt state*. Narad plainly has nothing to do with identifying the condition in which each individual processor of a system has exited an interrupt mode. At best, Narad discloses a set of semaphores bit that indicate when one of the computer systems of Narad (a) is entering a sleep state; or (b) is in a sleep state. Narad's teaching of identifying when a *computer system* is entered or has entered a sleep state does not disclose or teach the claimed step of identifying when *each processor* of a computer system has exited an interrupt mode.

Because all of the elements of claims 1 and 15 are not shown by the combination of Goodman and Narad, the rejection of claims 1 and 15 on obviousness grounds should be withdrawn and these claims should be passed to issuance.

B. Independent Claim 8

Like independent claims 1 and 15, independent claim 8 has been rejected on the basis of the combination of Goodman and Narad. According to the Examiner, Narad supplies the teaching of a semaphore associated with the processors and the ability to negate the semaphore to indicate that a non-interrupt handling process has exited interrupt mode. As was the case with claims 1 and 15, the Examiner points to the following passage of Narad for the teaching of the negation of a semaphore to indicate the exit of a processor from interrupt mode:

> S_Sleep_Enter and S_Wakeup_Enable semaphore bits: the S_Sleep_Enter semaphore bit of the system controller provides an indicator that the computer system is in the process of entering the sleep state, and inhibits power up of the processor module(s) until the corresponding S_Wakeup_Enable semaphore bit is set. The setting of the S_Wakeup_Enable bit indicates that the processor module(s) of the computer system has completed the power-down sequence and it is now safe to initiate a power up of the processor module(s).
>
> Wakeup_Reset bit: a status bit of the system controller for indicating that the cause of reset signal is a wakeup of the computer system, as opposed to a system-wide power on reset.

(Narad, col. 4, lines 8-22). This passage of Narad makes no reference to the negation of a semaphore to indicate that a processor is exiting and interrupt mode. This passage only concerns the entry of a computer system into a sleep state and identification that the computer system has actually achieved the entry into a sleep state.

Because the elements of claim 8 are not shown by the combination of Goodman and Narad, a prima facie case of obviousness is not shown and the rejection of claim 8 on obviousness grounds should be withdrawn.

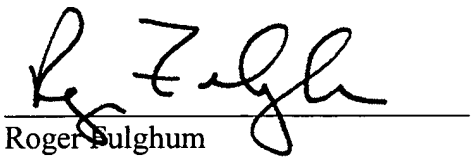
B. The Rejection of Dependent Claims 2-7, 9-14, and 16-20

The rejection of dependent claims 2-7, 9-14, and 16-20 will not be discussed individually herein, as each of these claims depends, either directly or indirectly, from an otherwise allowable base claim.

Conclusion

The applicant respectfully submits that the pending claims 1-20 of the present invention, as amended, are allowable. The applicant respectfully requests that the rejection of the pending claims be withdrawn and that these claims be passed to issuance.

Respectfully submitted,



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